Remarks

This Amendment is responsive to the **December 17, 2007** Office Action. Reexamination and reconsideration of the remaining claims (1-11, and 14-22) is respectfully requested.

Summary of The Office Action

Claims 17-19 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

Claims 17-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-3, 6-11, 14, and 17-20 were rejectec under 35 U.S.C. §103(a) as purportedly being unpatentable over Cooper et al. (US Patent No. 7,082,542) (Cooper) in view of Adachi (US Patent Appl. Pub. 2006/0041786 A1).

Claims 4-5, 15-16, and 22 were rejected under 35 U.S.C. 103(a) as purportedly being unpatentable over Cooper in view of Adachi, in view of Oshins et al. (US Patent No. 6,980,944 B1)(Oshins).

Claim 21 was rejected under 35 USC 103(a) as being unpatentable over Cooper in view of Adachi, in view of Bhatia et al. (US Patent No. 6,535,798 B1)(Bhatia).

Claim Interpretation

The Office Action states in a Claim Interpretation section (page 2) that the claim limitation "to produce a simulated processor performance state without causing an actual ACPI processor performance state change" is being interpreted as meaning "where the actual internal frequency of the processor has not been changed (Specification [0039], the free running clock 302 of Adachi) by throttling a clock signal supplied to the processor (Specification, [0061], clock throttling controller 312). While the internal state of the processor has not been changed, externally the state of the processor has changed, as the logic establishes the desired (simulated) processor performance state by causing the processor to be throttled (Specification [0060])." This interpretation is not completely accurate.

The claims specifically recite that no ACPI state change occurs. ACPI states are internal processor states that are associated with processor frequency. The interpretation provided by the Office Action makes an invalid distinction between internal ACPI states and external ACPI states. An external state simply would not be an ACPI state and therefore the interpretation lacks merit. Furthermore, the primary reference (Cooper), requires an explicit ACPI state change inside a processor. Thus, the interpretation is inconsistent with the primary reference.

Claims 17-19 Comply With 35 U.S.C. §112

35 U.S.C. §112

The Office Action asserts that independent claim 14 and dependent claims 17-19 are inconsistent because of limitations found in claims 17-19 that are contradictory to claim 14. This is incorrect. The claimed methods concern producing simulated processor states in response to receiving requests to produce actual processor performance states.

Claim 14 describes how a request to establish an actual processor performance state is received. Claim 14 then describes creating a simulated processor state without actually causing an ACPI processor performance state change. The simulated state that is produced may depend on the type of actual state requested.

Claims 17-19 describe the types of requests that can be received. Some requests may concern two processor states, while others concern two or more (e.g., eight) processor states. Regardless of the type of request received, all of claims 14 and 17-19 conclude with the method producing a simulated processor state. None of these claims include producing an actual processor performance state.

Thus, the rejection is without merit and Applicant respectfully requests that the rejection be withdrawn.

The Claims Patentably Distinguish Over the References of Record

35 U.S.C. §103

Claims 1-3, 6-11, 14, and 17-20 were rejected under 35 U.S.C. §103(a) as purportedly being unpatentable over Cooper in view of Adachi.

To establish a prima facie case of 35 U.S.C. §103 obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143.03 The teaching or suggestion to make the claimed combination must be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). This requirement is intended to prevent unacceptable "hindsight reconstruction" where Applicant's invention is recreated from references using the Application as a blueprint.

Here, the criterion described in MPEP 2143.03 is not satisfied since the references do not teach or suggest all the claim limitations. All the independent claims concern simulating a processor performance state without causing an actual ACPI processor performance state change. Cooper does not teach creating a simulated processor performance state without causing an actual ACPI processor performance state change. Instead, Cooper teaches a throttling emulator that requires an ACPI processor performance state change. None of the references cure this defect in Cooper. Thus, none of the claims are obvious for at least this reason.

Independent Claim 1

Claim 1 recites an apparatus that produces a simulated processor performance state without causing an actual ACPI processor performance state change. The Office Action asserts that claim 1 is obvious in light of Cooper and Adachi. However, Cooper does not teach simulating a processor performance state but rather teaches actually changing internal ACPI processor performance states.

Cooper recites that "[t]he processor is transitioned to one of the operational state and the low power state according to the processor state." (Abstract).

Furthermore, Cooper actually teaches away from the claimed apparatus. Cooper recites that "throttling ... has a number of drawbacks ... it is complicated ... requires complex external interface circuits ... is not compatible with software standards in power management ... is not efficient ... [and] is not flexible in generating an arbitrary duty cycle." Column 1, lines 22-28. No-one reading about these drawbacks would be motivated to attempt to simulate ACPI states using throttling. All the faults associated with throttling as described in Cooper reside in Adachi making it highly unlikely that one skilled in the art would be motivated to combine these references.

Having described the shortcomings associated with throttling, Cooper then describes an alternative known as "emulating throttling". Column 1, line 54. Emulating throttling includes "transitioning the processor to one of the operational state and the low power state." Column 1, lines 59-61. The throttling emulator includes a throttling state and an Advanced Configuration and Power Interface (ACPI) operating system. Column 4, lines 15-29. The throttling emulator transitions to a low power state by setting a processor to one of the ACPI states C1, C2, C3, and sleep state S1. Column 5, lines 31-39. The throttling emulator transitions to an operational power state by setting a processor to the ACPI state C0. Column 5, lines 40-46. Cooper recites that "the SMI timer handler performs operations to enter the desired low state (Block 440). As discussed above, the low state may be any one of a power state C1, C2, C3, and the sleep state S0. ... The SMI timer handler performs operations to enter the normal operational state (e.g., the C0 state) (block 450)". Column 6, lines 24-46. Cooper unquestionably involves an internal ACPI state change.

Cooper describes how emulating throttling involves changing an internal ACPI state. This is precisely the limitation that the claim language "without causing an actual ACPI processor performance state change" addresses. All the independent

claims require that no ACPI state change happen yet Cooper requires that an ACPI state change happen. Thus, Cooper is exactly opposite to the approach claimed and described. For at least this reason Cooper does not render any of the independent claims obvious.

The rejection of claim 1 is inconsistent with the incorrect claim interpretation provided on page 2 of the Office Action. The interpretation concerns the claim limitation "to produce a simulated processor performance state without causing an actual ACPI processor performance state change". The interpretation is that "the actual internal frequency of the processor has not been changed (Specification [0039], the free running clock 302 of Adachi) by throttling a clock signal supplied to the processor (Specification, [0061], clock throttling controller 312). While the internal state of the processor has not been changed, externally the state of the processor has changed, as the logic establishes the desired (simulated) processor performance state by causing the processor to be throttled (Specification [0060])." Yet Cooper describes how emulating throttling involves changing an internal ACPI state. This is the limitation that the claim language "without causing an actual ACPI processor performance state change" addresses. This is a limitation that appears inconsistent with the claim interpretation that recites that "externally the state of the processor has changed". In Cooper, an internal state has been changed. Therefore, it appears that Cooper cannot be applied as a reference in light of the claim interpretation. For at least this reason Applicant respectfully requests that the rejection be withdrawn and the claim be allowed.

The Office Action states that Cooper does not explicitly disclose producing the simulated processor performance state without causing an actual ACPI processor performance state change. But that is exactly what claim 1 describes, creating a simulated processor performance state without causing an actual ACPI processor performance state change. Cooper changes a state explicitly, the claim does not.

The Office Action attempts to remedy this defect in Cooper through the teachings of Adachi. Regardless of what Adachi shows, it would be impossible to simulate processor performance states using Cooper without causing the actual ACPI state change described in Cooper. No reference can overcome the fatal flaw in Cooper. The processor in Cooper transitions between an operational ACPI state and a low power ACPI state. The claimed apparatus causes no such ACPI state change. To the extent that any throttling occurred in Cooper, it would necessarily be accompanied by an ACPI state change. Therefore, Cooper, does not teach or suggest all the claim limitations as required by MPEP 2143.03 and thus the Office Action fails to establish a prima facie case of obviousness for claim 1. Claims 2-11 depend from claim 1 and are similarly not obvious.

The Office Action asserts that Adachi teaches producing a simulated processor performance state. (Page 4, paragraph 5) The Office Action relies on [0022], figure 3, and its accompanying text, and the free-running clock generator 302. The Office Action asserts that "the actual performance state of the processor never changes, but the simulated processor performance state changes due to the throttling of the throttled clock signal 307."

Adachi concerns "clock throttling in an integrated circuit." (Title, Abstract) Cooper explains why throttling is a bad idea. No-one would be motivated to combine the Adachi throttling reference with the anti-throttling Cooper reference. If the references were combined, Cooper would still require an internal state change, which is directly contradictory to the claim. Even though Adachi may describe throttling, that throttling can not possibly undo the internal state change performed by Cooper.

Thus, there is no possible motivation to combine Cooper and Adachi, and even if the references were combined, all the elements of the claim would not be taught because Cooper requires an internal state change. For at least this reason this claim is not obvious and is in condition for allowance. Accordingly, claims 2-11 are similarly not obvious and are in condition for allowance.

Dependent Claim 10

This claim depends from claim 1 and is not obvious for at least the same reasons as its parent claim. However, claim 10 recites the additional limitation of asserting a signal on the STPCLK# line. Cooper expressly teaches away from STPCLK# throttling when it recites that "STPCLK# throttling ... has a number of drawbacks ... it is complicated ... requires complex external interface circuits ... is not compatible with software standards in power management ... is not efficient ... [and] is not flexible in generating an arbitrary duty cycle." Column 1, lines 22-28. No-one could use Cooper to simulate processor states without causing an ACPI state change and furthermore, no-one reading about these drawbacks would be motivated to attempt to simulate ACPI states using STPCLK# throttling. Therefore claim 10 is not obvious for this additional reason.

Independent Claim 14

Claim 14 describes a method for causing a processor to operate as though an ACPI processor performance state has been established without actually causing an ACPI processor performance state change. As described above, Cooper requires an ACPI state change. Therefore, Cooper does not render claim 14 obvious. Claims 15-21 depend from claim 14 and are similarly not obvious.

Adachi, cannot possibly remedy the defect of Cooper. Additionally, no reference can possibly remedy the defect of Cooper. While Adachi describes thermal management by clock throttling, that throttling, when combined with Cooper, still produces the explicit state change produced by Cooper. Therefore, the combination of Cooper and Adachi does not render claim 14 obvious. Accordingly, the combination of references does not render claims 15-21 obvious.

Dependent Claim 20

This claim depends from claim 14 and is not obvious for at least the same reasons as its parent claim. However, claim 20 recites the additional limitation of

asserting a signal on the STPCLK# line. Cooper expressly teaches away from STPCLK# throttling when it recites that "STPCLK# throttling ... has a number of drawbacks ... it is complicated ... requires complex external interface circuits ... is not compatible with software standards in power management ... is not efficient ... [and] is not flexible in generating an arbitrary duty cycle." Column 1, lines 22-28. No-one could use Cooper and Adachi to simulate processor states without causing an ACPI state change and furthermore, no-one reading about these drawbacks would be motivated to attempt to simulate ACPI states using STPCLK# throttling. Therefore claim 20 is not obvious for this additional reason.

Claims 4-5, 15-16, and 22 were rejected under 35 U.S.C. 103(a) as purportedly being unpatentable over Cooper in view of Adachi, and further in view of Oshins.

Claims 4-5 depend from claim 1, which has been shown to be not obvious due to the overwhelming deficiency of Cooper as a reference. As described above, Cooper requires an internal state change while the claims explicitly call out not producing an internal state change. Adachi, while producing no internal state change to a free running clock 302, does not undo the internal state change required by Cooper. Therefore, the combination of Cooper and Adachi does not render these claims obvious. Oshirs does not remedy the defects of the Cooper/Adachi combination.

The Office Action asserts that Oshins teaches memory storing an ACPI table operably connected to a BIOS. This is correct. However, Oshins does not overcome the defect of Cooper. The combination of Cooper, Adachi, and Oshins would still cause an explicit internal state change, which is directly contrary to the claims. For at least this reason these claims are not obvious and are in condition for allowance.

Claims 15-16 recite establishing the data structure as an ACPI table in a BIOS. Oshins illustrates the ACPI tables 222 being external to ACPI BIOS 220 and to BIOS 26. Therefore, Oshins does not teach the additional claimed element. For this additional reason these claims are not obvious and are in condition for allowance.

Claim 22 describes a computer-readable medium that stores instructions that cause a processor to perform a method. The method includes causing a processor performance state to be simulated without causing an actual ACPI state change. As described above, Cooper requires an ACPI state change. Therefore Cooper does not render claim 22 obvious. Neither Adachi nor Oshins remedy the defect of Cooper. Additionally, claim 22 recites establishing an ACPI table in a BIOS. Oshins teaches establishing an ACPI table 222 outside of ACPI BIOS 220 or BIOS 26. For at least this additional reason this claim is not obvious and is in condition for allowance.

Claim 21 was rejected under 35 USC 103(a) as being unpatentable over Cooper in view of Adachi, and further in view of Bhatia. As described above, Cooper teaches an explicit change of an internal state. Neither Adachi nor Bhatia remedy this defect since neither "undoes" the explicit state change required by Cooper. Thus, claim 21 is not obvious over the combination of references and is in condition for allowance.

Conclusion

For the reasons set forth above, **claims 1-11 and 14-22** patentably and unobviously distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,

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